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10/677,850	10/02/2003	Jeffrey Raynor	03EDI22652634	5132

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EXAMINER
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SINES, BRIAN J

ART UNIT	PAPER NUMBER
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1797

NOTIFICATION DATE	DELIVERY MODE
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06/16/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

creganoa@addmg.com

## **ADVISORY ACTION**

### ***Response to Arguments***

Applicant's arguments filed 5/30/2008 have been fully considered but they are not persuasive.

The prior art teachings are still considered to meet the limitations and are within the scope of the claimed invention. In other words, the claims still do not *exclude* the methodology taught by the prior art. The recitation of the “integrated circuit die” is still not considered to be supported the specification. Nevertheless, Venkat still teaches that the sensor comprises an optical sensor “IC,” which is an “integrated chip” (see, e.g., col. 1, lines 6 – 29). As indicated by the Applicant, a “die” in this art, at the least, can be interpreted as a structure comprising a circuit supported on a semiconductor wafer substrate that is collectively considered a “chip.” The claim language of the instant claims do not exclude the teachings of Venkat with regard to this particular feature. Giving a broad and reasonable interpretation to the claim term of art “integrated circuit,” and including an “integrated circuit die,” the prior art still meets this limitation. With regards to the recitation of a “flip-chip arrangement,” the prior art teachings are still considered to meet this limitation. This recitation merely describes a mounting configuration wherein the chip is bump bonded face down with a substrate (see Applicant’s specification, paragraph 11). As shown in figure 2 of Venkat, the optical IC 32 is positioned “face down” with respect to a mounting substrate, e.g., 36. Giving a broad and reasonable interpretation to this claim term of art, this claim term interpretation is not limited to any particular type of secure bonding attachment, i.e., wire bonding or bump bonding. The claim

language still does not *exclude* the teachings of the prior art with regards to this particular feature.

It is well settled that the United States Patent and Trademark Office (PTO) is obligated to give a disputed claim term its broadest reasonable interpretation, taking into account any enlightenment by way of definitions or otherwise found in the specification. See *In re Bigio*, 381 F.3d 1320, 1324, 72 USPQ2d 1209, 1211 (Fed. Cir. 2004) (“[T]he PTO gives a disputed claim term its broadest reasonable interpretation during patent prosecution.”). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); *In re Barr*, 170 USPQ 330 (CCPA 1971). The applicant cannot read limitations set forth in the description into the claims for the purpose of avoiding the art. See *In re Sporck*, 155 USPQ 687 (CCPA 1967). The claims must be given their broadest reasonable interpretation consistent with the supporting description. See *In re Hyatt*, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). “The PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art.” See *In re Morris*, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997). “During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow.” See *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). “The PTO broadly interprets claims during examination of a patent application since the applicant may ‘amend his claim to obtain protection commensurate with his actual contribution to the art.’”(quoting *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550 (CCPA 1969)). See *In re Yamamoto*, 740 F.2d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984).

See the final Office action mailed 4/1/2008.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Sines whose telephone number is (571) 272-1263. The examiner can normally be reached on Monday - Friday (11 AM - 8 PM EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jill A. Warden can be reached on (571) 272-1267. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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